Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1.   (currently amended) An integrated circuit, comprising:

at least one processing unit (PU);

a cache memory (L2_bank) having a plurality of memory modules for caching data;

remapping means (RM, MapRAM) for performing an unrestricted remapping within said plurality of memory modules, wherein the unrestricted remapping permits remapping the memory modules from a first _physical_ bank of memory modules to a second _physical_ bank of memory modules.

2.   (previously presented) The integrated circuit according to claim 1, wherein said cache memory (L2_BANK) is a set-associative cache.

3.   (previously presented) The integrated circuit according to claim 1, wherein said remapping means is adapted to perform the remapping on the basis of a programmable permutation function.

4.   (previously presented) The integrated circuit according to claim 1, wherein said remapping means is adapted to perform the remapping on the basis of a reduction mapping, wherein the reduction mapping performs the remapping using less output symbols than input symbols.

5.   (previously presented) The integrated circuit according to claim 1, further comprising:

a Tag RAM unit (TagRAM) associated to said cache for identifying which data is cached in said cache memory (L2_BANK), and

wherein said remapping means is arranged in series with said Tag RAM unit (TagRAM).

6.   (previously presented) The integrated circuit according to claim 1, further comprising:

a Tag RAM unit (TagRAM) associated to said cache for identifying which data is cached in said cache memory (L2_BANK), and

wherein said remapping means is arranged in parallel to said Tag RAM unit (TagRAM).

7.   (previously presented) The integrated circuit according to claim 5, further comprising:

a look up table for marking faulty memory modules.

8.   (currently amended) A method of cache remapping in an integrated circuit having at least one processing unit (PU); a main memory (MM) for storing data; and a cache memory (L2_BANK) having a plurality of memory modules for caching data, the method comprising:

performing an unrestricted remapping within said plurality of memory modules, wherein the unrestricted remapping permits remapping the memory modules from a first physical bank of memory modules to a second physical bank of memory modules.

9.   (previously presented) The integrated circuit according to claim 1, wherein the remapping means is further configured to distribute faulty memory modules evenly over a plurality of banks.

10. (previously presented) The integrated circuit according to claim 1, wherein the remapping means is further configured to perform the unrestricted remapping at a block/line granularity of the memory modules.

11. (currently amended) The integrated circuit according to claim 1, wherein the remapping means is further configured to remap at least one of the memory modules from an index within the first physical bank of memory modules to a new way and a different index within the second physical bank of memory modules.

12. (new) The integrated circuit according to claim 1, wherein said cache memory comprises a plurality of dynamic random access memory (DRAM) modules.

13. (new) The integrated circuit according to claim 1, wherein the remapping means is further configured to remap at least one of the memory modules to a new way and a same index within the second physical bank of memory modules.

14. (new) The method of cache remapping according to claim 8, further comprising performing the unrestricted remapping on the basis of a reduction mapping using less output symbols than input symbols.

15. (new) The method of cache remapping according to claim 8, further comprising marking faulty memory modules in a look up table.

16. (new) The method of cache remapping according to claim 8, wherein said cache memory comprises a plurality of dynamic random access memory (DRAM) modules.

17. (new) The method of cache remapping according to claim 8, further comprising remapping at least one of the memory modules to a new way and a same index within the second physical bank of memory modules.

18. (new) The method of cache remapping according to claim 8, further comprising remapping at least one of the memory modules to a new way and a different index within the second physical bank of memory modules.